REMARKS

I. Formalities

Claims 1-9 and 18-32 have been elected herein, without traverse.

II. Response to the Restriction Requirement

A restriction of Applicant's claims was required under 35 U.S.C. §121 for the following groups of claims:

I. Claims 1-9 and 18-24, drawn to a semiconductor device, classified in class 257, subclass 675 or a system classified in class 700, subclass 90; and

II. Claims 10-17, drawn to a process of making a semiconductor device, classified in class 438, subclass 109.

For convenience, a listing of the pending claims is given below. Applicant respectfully draws the examiner's attention to the fact that certain amendments are proposed to the elected claims 1 and 18 and to the fact that new claims 25-32 are also proposed herein. Applicant also proposes to cancel claims 10-17.

Support for the amendments to claims 1 and 18 can be found at least in paragraph [0022] and in FIGs. 3 and 4 of the originally-filed patent application.Support for the new claims can also be found at least in paragraph [0022] and in FIGs. 3 and 4 and also in paragraph [0019].

As required by the Office Action, Applicant elects to prosecute the claims of Group I, i.e., claims 1-9 and 18-24. New claims 25-32 are believed to fall within the same group and are also elected.

AMENDMENTS TO THE CLAIMS

In accordance with 37 C.F.R. §1.121(c), please amend the claims as indicated in marked-up form below, where additions are underlined, deletions are struck through, and new claims are presented without markings.

1. (Currently Amended) ~~An apparatus~~ A microelectronic device comprising:

a package substrate having a first side and an opposing second side; ~~including an integrated circuit disposed on two or more electrically coupled die, the first die including~~

a microprocessor adjacent to the first side of the package substrate ~~and the second die including a memory device~~; and

a memory device adjacent to the second side of the package substrate, wherein the package substrate is ~~a substrate of the package including one selected from the group consisting of a Land Grid Array, a Pin Grid Array, and a combination thereof~~ electrically coupled to at least one of the ~~die~~ microprocessor and the memory device.

2. (Original) The apparatus of Claim 1, further comprising a memory controller electrically coupled to the memory device.

3. (Original) The apparatus of Claim 1, further comprising a thin film capacitor integral to the substrate.

4. (Original) The apparatus of Claim 1, the second die disposed on a land side of the substrate.

5. (Original) The apparatus of Claim 1, further comprising a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.

6. (Original) The apparatus of Claim 5, the second die electrically coupled by one selected from the group including a wirebond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.

7. (Original) The apparatus of claim 1 further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.

8. (Original) The memory device of Claim 7 further comprising a fourth level cache.

9. (Original) The apparatus of Claim 1, the package further including an integrated heat spreader thermally coupled to one or more of the die.

10-17. (Canceled)

18. (Currently Amended) A system comprising:

a package including an integrated circuit disposed on two or more electrically coupled die, the first die including a microprocessor and the second die including a memory device;

a system memory bus coupled to the microprocessor;

a package substrate ~~of the package including one selected from the group consisting of a Land Grid Array, a Pin Grid Array, and a combination thereof~~ electrically coupled to at least one of the die; and

a mass storage device coupled to the package, wherein the memory device has a speed that exceeds a speed of the system memory bus.

19. (Original) The system of Claim 18 wherein the memory device further comprises a fourth level cache.

20. (Original) The system of claim 18, further comprising:

a dynamic random access memory coupled to the integrated circuit; and

an input/output interface coupled to the integrated circuit.

21. (Original) The system of claim 20, wherein the input/output interface comprises a networking interface.

22. (Original) The system of claim 18, wherein the system is a selected one of a group comprising a set-top box, a media-center personal computer, a digital versatile disk player, a server, a personal computer, a mobile personal computer, a network router, and a network switching device.

23. (Original) The system of claim 18, the memory device disposed in a recess formed by a land grid array socket, the package electrically coupled to the land grid array connector.

24. (Original) The system of claim 23, the land grid array connector coupled to a printed circuit board assembly capable of further coupling to a motherboard.

25. (New) The microelectronic device of claim 8, wherein the fourth level cache has a capacity ranging between approximately 500 megabytes and approximately 1 gigabyte.

26. (New) The microelectronic device of claim 25 further comprising a system memory bus coupled to the microprocessor, wherein the fourth level cache has a speed greater than a speed of the system memory bus.

27. (New) The microelectronic device of claim 1 further comprising a land grid array connector coupled to the package substrate.

28. (New) The microelectronic device of claim 1 further comprising a pin grid array connector coupled to the package substrate.

29. (New). A microelectronic device comprising:

a package substrate;

a microprocessor coupled to the package substrate; and

a memory device coupled to the package substrate, wherein the memory device comprises a fourth level cache.

30. (New) The microelectronic device of claim 29 wherein:

the fourth level cache has a capacity ranging between approximately 500 megabytes and approximately 1 gigabyte.

31. (New) The microelectronic device of claim 30 further comprising:

a third level cache and a system memory bus,

wherein:

the fourth level cache has a speed greater than a speed of the system memory bus; and

the capacity of the fourth level cache is greater than a capacity of the third level cache.

32. (New) The microelectronic device of claim 31 further comprising one of a land grid array connector and a pin grid array connector coupled to the package substrate.

CONCLUSION

No fees are believed to be due with this Response. However, the Commissioner for Patents is hereby authorized to charge any fees due, or credit any overpayment, to Account No. 50-0221.

If there are matters that can be discussed by telephone to further the prosecution of this application, Applicant invites Examiner Nguyen to call the undersigned attorney at the Examiner's convenience.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited either via facsimile or via the United States Postal Service addressed to: MS Amendment, United States Patent and Trademark Office, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3 day of August 2009.

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